

August 1999

# FDN342P

### P-Channel 2.5V Specified PowerTrench™ MOSFET

### **General Description**

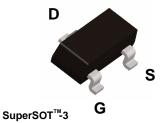
This P-Channel 2.5V specified MOSFET is produced in a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications for a wide range of gate drive voltages (2.5V - 12V).

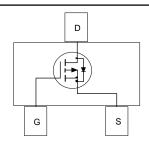
### **Applications**

- · Load switch
- · Battery protection
- · Power management

### **Features**

- -2 A, -20 V.  $R_{DS(ON)} = 0.08~\Omega$  @  $V_{GS} =$  -4.5 V  $R_{DS(ON)} = 0.13~\Omega$  @  $V_{GS} =$  -2.5 V.
- Rugged gate rating (±12V).
- High performance trench technology for extremely low  $R_{\mbox{\tiny DS(ON)}}.$
- Enhanced power SuperSOT™-3 (SOT-23).





### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units	
V <sub>DSS</sub>	Drain-Source Voltage	-20	V	
V <sub>GSS</sub>	Gate-Source Voltage	±12	V	
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	-2	A
	- Pulsed		-10	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperatu	-55 to +150	°C	

### **Thermal Characteristics**

$R_{_{\theta}JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
R <sub>o</sub> JC	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

**Package Outlines and Ordering Information** 

Device Marking	Device	Reel Size	Tape Width	Quantity	
FDN342P	FDN342P	7"	8mm	3000 units	

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics		•			
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A,Referenced to 25°C		-16		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V			-1	μΑ
GSSF	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 12 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -12 V, V <sub>DS</sub> = 0 V			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-0.6	-1.05	-1.5	V
$\Delta V_{GS(th)} = \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A,Referenced to 25°C		3		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2 A V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2 A,T <sub>J</sub> =125°C V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1.5 A		0.062 0.086 0.099	0.08 0.14 0.13	Ω
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -5 V	-5			Α
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -5 A		7		S
Dvnamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -10 \ V, V_{GS} = 0 \ V$		635		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		175		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			75		pF
Switchin	g Characteristics (Note 2)					•
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -1 A		20	35	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		8	16	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	1		9	18	ns
t <sub>f</sub>	Turn-Off Fall Time	7		19	32	ns
Qg	Total Gate Charge	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -2 A		6.3	9	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{GS} = -4.5 V$ ,		1.5		nC
Q <sub>gd</sub>	Gate-Drain Charge			1.7		nC
Drain-So	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source				-0.42	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -0.42 \text{ A}$ (Note 2)		-0.7	-1.2	V

#### Notes

 $\mathbf{1}.R_{\text{eJA}}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\text{eJC}}$  is guaranteed by design while  $R_{\text{eCA}}$  is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. Cu.



b) 270°C/W when mounted on a mininum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%

## **Typical Characteristics**

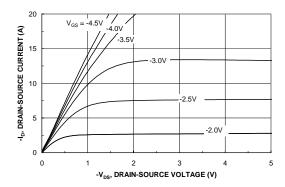


Figure 1. On-Region Characteristics.

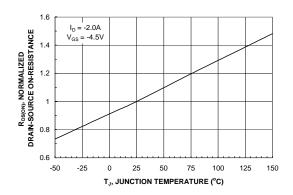


Figure 3. On-Resistance Variation with Temperature.

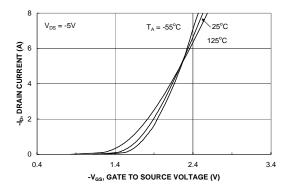


Figure 5. Transfer Characteristics.

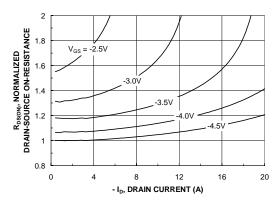


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

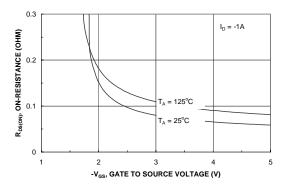


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

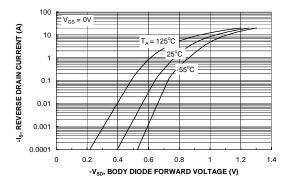
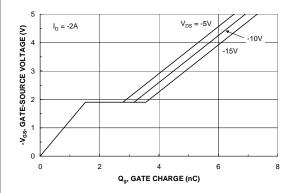


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics (continued)



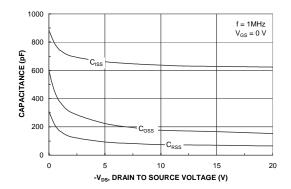
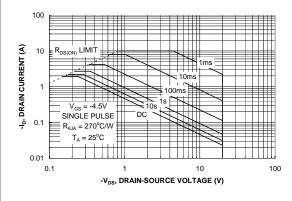


Figure 7. Gate Charge Characteristics.





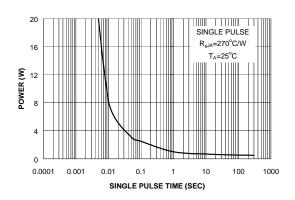


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

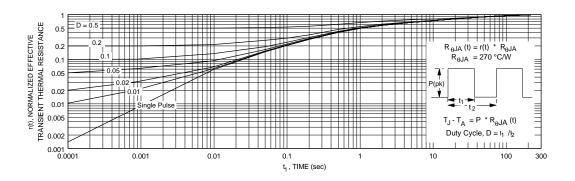
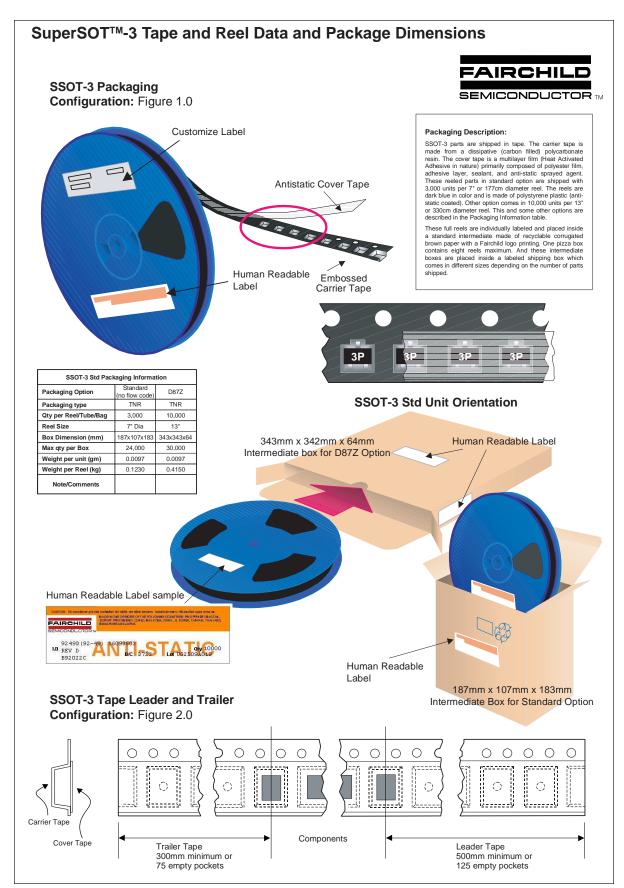


Figure 11. Transient Thermal Response Curve.

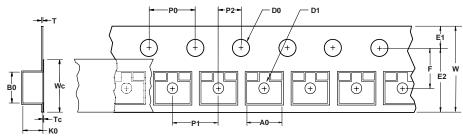
Thermal characterization performed using the conditions described in Note 1b. Transient themal response will change depending on the circuit board design.

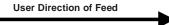




### SSOT-3 Embossed Carrier Tape

Configuration: Figure 3.0



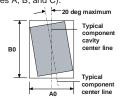


	Dimensions are in millimeter													
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SSOT-3 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-02

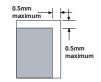
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

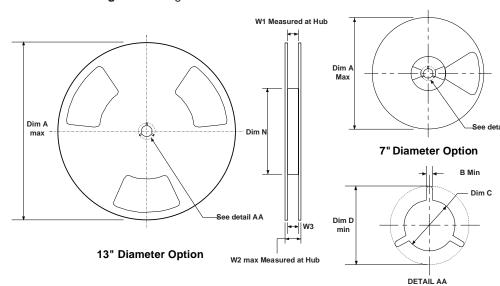


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

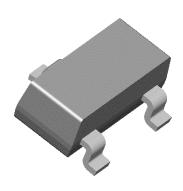
### SSOT-3 Reel Configuration: Figure 4.0

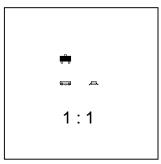


	Dimensions are in inches and millimeters								
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

# SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

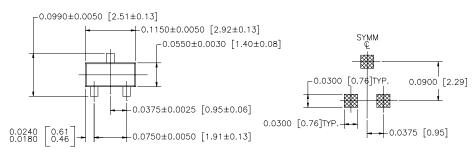
# SuperSOT™-3 (FS PKG Code 32)



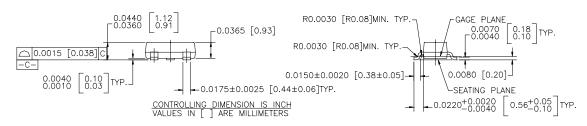


Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0097



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

SUPER SOT , 3 LEADS

- 1. STANDARD LEAD FINISH TO BE 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.
- 2. NO JEDEC REGISTRATION AS OF DEC. 1995.

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E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

 $\begin{array}{lll} \mathsf{FACT} \ \mathsf{Quiet} \ \mathsf{Series^{\mathsf{TM}}} & \mathsf{Quiet} \ \mathsf{Series^{\mathsf{TM}}} \\ \mathsf{FAST}^{\otimes} & \mathsf{SuperSOT^{\mathsf{TM}}}\text{-}3 \\ \mathsf{FASTr^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}}\text{-}6 \\ \mathsf{GTO^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}}\text{-}8 \\ \mathsf{HiSeC^{\mathsf{TM}}} & \mathsf{TinyLogic^{\mathsf{TM}}} \\ \end{array}$ 

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